Applicants provide a marked-up version of the amended claims in an attached Appendix designated "Version of Claims with Markings to Show Changes Made." The amendments to the claims do not include any new matter. Claims 30 – 38 are pending.

Regarding the Office Action:

In the Office Action, the Examiner objected to the drawings and required "corrected drawings" as one option to overcome the objection (Office Action, p. 2); objected to the Specification because of the Abstract of the disclosure; rejected claims 30 – 36 under 35 U.S.C. § 112, 2nd paragraph as indefinite; rejected claims 37 and 38 under 35 U.S.C. § 112, 2nd paragraph as indefinite; rejected claims 30 – 36 under 35 U.S.C. § 102(e) as anticipated by Hsu, et al. (U.S. Patent No. 5,482,888); and rejected claims 37 and 38 under 35 U.S.C. § 102(e) as anticipated by "Applicant's Prior Art (Fig. 2b)" (Office Action, p. 5).

Applicants respectfully traverse the objections and rejections, as detailed above, for the following reasons.

Regarding the Objection to the Drawings:

The Examiner objected to the drawings under 37 C.F.R. §§ 1.83(a) and 1.84(p)(4) (Office Action, p. 2). In particular, the Examiner alleged that claimed features were not shown in the drawings (37 C.F.R. §§ 1.83(a) objection), and that "reference character "6" has been used to designate both diffusion layer and silicide in Fig. 2b" (Office Action, p. 2) (37 C.F.R. §§ 1.84(p)(4) objection).

Regarding Fig. 16X:

Applicants propose amending Fig. 16X, to correct the fact that reference numerals 113 and 137 inadvertently designated the same component. Also, reference numerals 113, 132, and 135 were added to more clearly show in the drawings what is already described in the

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

specification. The corrections are shown in red ink on the attached Request for Approval of Drawing Changes. Upon approval of the proposed changes, Applicants respectfully request that the submission of formal revised drawings be deferred until after issuance of a Notice of Allowance.

Regarding the 37 C.F.R. §§ 1.83(a) Objection:

Applicants submit that Figs. 3K and 16X are examples (not exclusive) of the first to thirteenth embodiments, as claimed in independent claim 30. These drawings illustrate, for example, gate electrode (25, 113), gate wiring layer (25, 113), source electrode (22, 135), and drain electrode (22, 135), having upper surface levels equal to or lower than an upper surface level of the device isolation insulating film (16, 106). Using these drawings as an example of an embodiment only, Applicants' claimed device of independent claim 30 can obtain advantages, for example, as described in the specification on p. 38, l. 18 to p. 39, l. 9.

Furthermore, in Fig. 3K, *in* the component designated by reference numeral 25, a portion located between the source and drain electrodes 22 corresponds to a gate electrode, and the rest of the component corresponds to a gate wiring layer. In the same manner, in Fig. 16X, *in* the component designated by reference numeral 113, a portion located between the source and drain electrodes 135 corresponds to a gate electrode, and the rest of the component corresponds to a gate wiring layer. This can be readily understood by one skilled in the art, in view of Applicants' independent claim 30 reciting elements such as "gate electrode" and "gate wiring layer," for example, and further in view of the description in Applicants' specification on p. 20, ll. 13 – 16.

In addition, Applicants submit that Fig. 3K is an example (not exclusive) of the fourteenth and fifteenth embodiments, as claimed in independent claim 37. Fig. 3K illustrates, for example, a pair of thin films 204 formed by epitaxial growth of a semiconductor on one

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

major surface of the substrate 201, and arranged on two sides of the gate wiring layer 212. Fig. 3K also illustrates, for example, a gate sidewall 207 formed on the pair of thin films 204, covering the side surface of the gate wiring layer 212, and made of an insulator. Using this drawing as an example of an embodiment only, Applicants' claimed device of independent claim 37 can obtain the advantages described in the specification on p. 73, l. 25 to p. 74, l. 6.

Finally, to counter the Examiner's allegations that claimed features were not shown in the drawings, and in light of the discussion above, Applicants therefore submit that Figs. 3K and 16X, among other drawings, illustrate at least an element of independent claim 30, in that "an insulation film [24, 132] covering bottom and side surfaces of each of said gate electrode [25, 113] and said gate wiring layer [25, 113]." Figs. 3K and 16X, among other drawings, also illustrate at least an element of independent claim 30, in that "a gate wiring layer [25, 113] formed in said device isolation insulating film [16, 106] and connected to said gate electrode [25, 113]." Fig. 16X, among other drawings, illustrates at least an element of claim 32, in that "said gate electrode [113] and said gate wiring layer [113] have bottom surfaces lower than upper surfaces of said source and drain diffusion layers [130]." Fig. 3K, among other drawings, illustrates at least an element of claim 33, in that "said gate electrode [25], said gate wiring layer [25], said source electrode [22], and said drain electrode [22] have upper surface levels equal to each other." Figs. 15A – 15D, among other drawings, also illustrate at least an element of independent claim 36, in that "a connection wiring layer [158] connected to at least one of said source electrode [152, 153], said drain electrode [152, 153], said gate electrode [155], and said gate wiring layer [155], said connection wiring layer [158] having an upper surface level equal to or lower than the upper surface level of said device isolation insulating film [154]."

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

In light of the above discussion, Applicants therefore submit that all structures indicated by the Examiner are shown in the drawings and deem this objection overcome.

Regarding the 37 C.F.R. §§ 1.84(p)(4) Objection:

In response to this objection, Applicants point out that it is clear from the description in the specification, on p. 4, ll. 1 – 5, that Fig. 2B shows a structure prior to metal silicide layer formation. Furthermore, as is clear from the description in the specification, on p. 2, ll. 1 – 4, and from the description in the specification, on p. 4, ll. 3 – 5, that the metal silicide layer is formed by applying the SALICIDE method to the structure shown in Fig. 2B. The surface region of the n-type impurity diffusion region 6 shown in Fig. 2B is used as a part of the material of the metal silicide layer.

In light of this, Applicants deem the Examiner's allegation (that "reference character "6" has been used to designate both diffusion layer and silicide in Fig. 2b" (Office Action, p. 2)) erroneous, and therefore request the Examiner withdraw this objection to the drawings.

Regarding the Objection to the Abstract:

The Examiner objected to Applicants' Abstract because "it discloses the method of manufacturing a semiconductor device and the invention being claimed is a semiconductor device" (Office Action, p. 3), and required correction. Applicants have amended the Abstract to comply with the Examiner's required correction, and accordingly deem this objection overcome.

Applicants point out for the record that "[t]he abstract will not be used for interpreting the scope of the claims." *See* 37 C.F.R. § 1.72(b). Applicants attach a Substitute Abstract in clean form on a separate page. No new matter has been introduced, in accordance with the requirements of 37 C.F.R. § 1.121(f).

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Regarding the Rejection of Claims 30 – 36 under 35 U.S.C. § 112, 2nd paragraph:

Applicants refer the Examiner to exemplary portions of Applicants' specification to provide illustrative descriptions of Applicants' claimed invention, as indicated below.

The Examiner first alleged that

> "[c]laims 30 – 36 disclose an insulating layer formed on the bottom surface and side surface of the gate wiring layer, it is unclear how that is suppose[d] to be formed since the drawings do not disclose this limitation, the gate electrode, gate wiring layer, source and drain electrodes having an upper surface lower than or equal to the upper surface of the device isolation insulating film..." (Office Action, p. 3).

In response, Applicants direct the Examiner's attention to Figs. 3K, 16X, and to the description in the previous section, for example, which disclose the elements of Applicants' claims 30 – 36.

Second, the Examiner alleged that "it is unclear how the gate wiring layer is going to have an upper surface equal to or lower than the device isolation film if it is connected to the device isolation film..." (Office Action, p. 3). In response, Applicants point out that claims 30 – 36 do *not* recite the element "a gate wiring layer *connected to* the device isolation insulating film" (Office Action, p. 3, italics added), but instead recite "a gate wiring layer *formed in* said device isolation insulating film" (claim 30, italics added).

Third, the Examiner alleged that "it is unclear how the gate wiring layer and the gate electrode have a bottom surface lower than the source and drain diffusion layers since the drawings do not disclose this limitation and how is the wiring layer having a bottom surface lower if it is formed on the device isolation and the gate electrode..." (Office Action, p. 3). In response, Applicants point out that claims 30 – 36 do *not* recite the element "a gate wiring layer

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

formed on the device isolation insulating film *and the gate electrode*" (Office Action, p. 3, italics added), but instead recite "a gate wiring layer *formed in* said device isolation insulating film" (claim 30, italics added).

Fourth, the Examiner alleged that "it is also unclear how the gate electrode, gate wiring and source and drain electrodes could have upper levels equal to each other if the gate wiring layer is formed on the gate electrode it would always be higher than the gate electrode..." (Office Action, p. 4). In response, Applicants point out that claims 30 – 36 do *not* recite the element "a gate wiring layer *formed on* the gate electrode" (Office Action, p. 4, italics added), but instead recite "a gate wiring layer *formed in said device isolation insulating film and connected to* said gate electrode" (claim 30, italics added).

Fifth, the Examiner alleged that "it is unclear how the connection wiring is formed on ... either the gate electrode, gate wiring layer or source and drain electrodes and have an upper surface equal to or lower than the device isolation layer..." (Office Action, p. 4). In response, Applicants point out that claims 30 – 36 do *not* recite the element "connection wiring *formed on* ... either the gate electrode, gate wiring layer or source and drain electrodes" (Office Action, p. 4, italics added), but instead recite "a connection wiring layer *connected to* at least one of said source electrode, said drain electrode, said gate electrode, and said gate wiring layer" (claim 36, italics added). In addition, Fig. 15C, for example, illustrates connection wiring layer 158 connected to gate wiring layer 155.

Applicants further direct the Examiner to the exemplary citations to Applicants' specification, claims and drawings, made above, demonstrating that Applicants' claims 30 – 36 comply with 35 U.S.C. §112, 2nd paragraph. Applicants point out that

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

"[t]hey can define in the claims what they regard as their invention essentially in whatever terms they choose so long as the terms are not used in ways that are contrary to accepted meanings in the art. [They] may use ... any style of expression or format of claim which makes clear the boundaries of the subject matter for which protection is sought." M.P.E.P. § 2173.01, p. 2100-198.

In light of the above explanation, Applicants traverse the Examiner's five allegations that "it is unclear" (Office Action, pp. 3 – 4), and respectfully remind the Examiner that

> "[s]ome latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the examiner might desire. Examiners ... should not reject claims or insist on their own preferences if other modes of expression selected by applicants satisfy the statutory requirement." M.P.E.P. § 2173.02, 8th Ed., Rev. 1 (Feb. 2003), p. 2100-198 – 2100-199.

Applicants therefore respectfully deem the rejection of claims 30 – 36 overcome. Claims 30 – 36 fully comply with the requirements of 35 U.S.C. § 112, 2nd paragraph, and Applicants accordingly request withdrawal of the rejection.

Regarding the Rejection of Claims 37 and 38 under 35 U.S.C. § 112, 2nd paragraph:

Applicants refer the Examiner to exemplary portions of Applicants' specification to provide illustrative descriptions of Applicants' claimed invention, as indicated below.

The Examiner alleged that "[c]laims 37 and 38 disclose a pair of thin films formed on the sides of the gate wiring layer, it is unclear what the thin films are or what they are made of and in addition the claimed limitation as shown in the drawings is etched away so therefore there is not thin film in the final product" (Office Action, p. 4).

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

In response, Applicants point out that claim 37 recites, among other things, "a pair of thin films formed by epitaxial growing a semiconductor on one major surface of said substrate." Specifically, the thin films are "made of" the epitaxially grown semiconductor. Furthermore, Applicants direct the Examiner's attention to Fig. 22K, for example (not exclusive), illustrating each of the thin films is constituted by the component designated by reference numeral 204 and an upper portion of the component designated by reference numeral 208. Specifically, the thin films also exist in the final device as claimed.

In light of the above explanation, Applicants traverse the Examiner's allegations respectfully direct the Examiner to the above-quoted M.P.E.P. citations. Applicants further direct the Examiner to the exemplary citations to Applicants' specification, claims and drawings, made above, demonstrating that Applicants' claims 37 and 38 comply with 35 U.S.C. §112, 2nd paragraph.

Applicants therefore respectfully deem the rejection of claims 30 – 36 overcome. Claims 30 – 36 fully comply with the requirements of 35 U.S.C. § 112, 2nd paragraph, and Applicants accordingly request withdrawal of the rejection.

Regarding the Rejection of Claims 30 – 36 under 35 U.S.C. § 102(e):

Applicants respectfully traverse the rejection of claims 30 – 36 under 35 U.S.C. § 102(e) as anticipated by Hsu. In traversing the rejection, and while not admitting its propriety, Applicants note for the record that the Examiner applied the incorrect statutory subsection of 35 U.S.C. § 102 in the present rejection. Applicants assume the Examiner meant to rely on 35 U.S.C. § 102(b), and still traverse the rejection regardless of the statutory subsection applied. Should the Examiner maintain the rejection after consideration of these arguments, Applicants request the Examiner confirm the grounds of the rejection and the proper statutory subsection.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

In order to properly establish that Hsu anticipates Applicants' claimed invention under 35 U.S.C. § 102, each and every element of each of the claims in issue must be found, either expressly described or under principles of inherency, in that single reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131, 8th Ed., Rev. 1 (Feb. 2003), p. 2100-70, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Regarding the 35 U.S.C. § 102(e) rejection, Hsu does not teach each and every element of Applicants' present invention as claimed.

The Examiner incorrectly alleged that Hsu's Fig. 2H teaches each and every element of Applicants' claimed invention (Office Action, p. 5). In contrast, however, Applicants note that Hsu does not disclose at least Applicants' claimed "said gate electrode, said gate wiring layer, said source electrode, and said drain electrode have upper surface levels equal to or lower than an upper surface level of said device isolation insulating film" (claim 30). It is clear from Hsu's Fig. 2H, for example, that contact electrode 60, electrode 62, and electrode 67 all have upper surface levels *above* field oxide (FOX) 54. *See* Hsu, for example, col. 5, l. 64 – col. 6, l. 60.

Thus, since Hsu does not disclose each and every element of Applicants' independent claim 30, Hsu does not anticipate Applicants' claimed invention. In addition to Hsu not anticipating the present invention, Hsu does not disclose an identical invention, let alone in as complete detail as contained in Applicants' independent claim 30. Applicants therefore submit that the Examiner has not met these essential requirements of anticipation for a proper 35 U.S.C. § 102(e) rejection.

Therefore, Applicants submit that independent claim 30 is allowable, for the reasons already argued above. In addition, dependent claims 31 – 36 are also allowable at least by virtue

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

of their dependence from allowable base claim 30. Therefore, Applicants respectfully submit that the improper 35 U.S.C. § 102(e) rejection of claims 30 – 36 should be withdrawn.

Regarding the Rejection of Claims 37 and 38 under 35 U.S.C. § 102(e):

Applicant respectfully traverses the rejection of claims 37 and 38 under 35 U.S.C. § 102(e) as anticipated by "Applicant's Prior Art (Fig. 2b)" (Office Action, p. 5).

There requirements for a proper 35 U.S.C. § 102(e) rejection have already been set forth. Regarding the 35 U.S.C. § 102(e) rejection, "Applicant's Prior Art (Fig. 2b)" ("APA") does not teach each and every element of Applicants' present invention as claimed.

Applicants note that Fig. 2B does not disclose at least "a pair of thin films formed by epitaxial growing a semiconductor on one major surface of said substrate, and arranged on two sides of said gate wiring layer" (claim 37), and that the reference numeral 5 in Fig. 2B is the surface region of the substrate, and is not formed by epitaxial semiconductor growth on the substrate.

Thus, since APA does not disclose each and every element of Applicants' independent claim 37, APA does not anticipate Applicants' claimed invention. In addition to APA not anticipating the present invention, APA does not disclose an identical invention, let alone in as complete detail as contained in Applicants' independent claim 37. Applicants therefore submit that the Examiner has not met these essential requirements of anticipation for a proper 35 U.S.C. § 102(e) rejection.

Therefore, Applicants submit that independent claim 37 is allowable, for the reasons already argued above. In addition, dependent claim 38 is also allowable at least by virtue of its dependence from allowable base claim 37. Therefore, Applicants respectfully submit that the improper 35 U.S.C. § 102(e) rejection of claims 37 and 38 should be withdrawn.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Conclusion:

In making various references to the specification and drawings set forth herein, it is understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments described in the specification and illustrated in the drawings. Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law. Applicants respectfully point out to the Examiner that "[e]ach claim must be separately analyzed and given its broadest reasonable interpretation in light of and consistent with the written description." M.P.E.P. § 2163(II)(A)(1), p. 2100-163.

In view of the foregoing remarks, Applicants request the Examiner's reconsideration of the application and submit that the objections and rejections detailed above should be withdrawn. For the reasons articulated herein, Applicants submit that claims 30 – 38 are allowable, for the reasons already argued above. Applicants therefore submit that pending claims 30 – 38 are in condition for allowance. A favorable action is requested.

Should the Examiner continue to dispute the patentability of the claims after consideration of this Amendment, Applicants encourage the Examiner to contact Applicants' undersigned representative by telephone to discuss any remaining issues or to resolve any misunderstandings.

Please grant any extensions of time under 37 C.F.R. § 1.136 required in entering this response. If there are any fees due under 37 C.F.R. § 1.16 or 1.17, which are not enclosed,

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

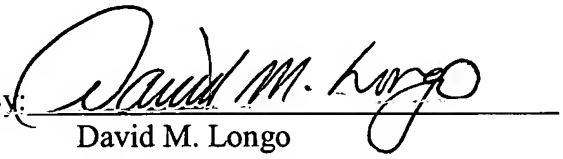
1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: June 30, 2003

By: 

David M. Longo
Reg. No. 53,235

/direct telephone: (202) 408–4489/

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

APPENDIX TO AMENDMENT of June 30, 2003

"VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE"

AMENDMENTS TO THE CLAIMS:

Please amend claim 30, 31, 36, and 37 as follows:

30. (Amended) A semiconductor device comprising:

a substrate;

a device isolation insulating film formed on one major surface of said substrate,

a gate electrode formed on [one] the major surface of said substrate;

a gate wiring layer formed [on] in said device isolation insulating film and connected to said gate electrode;

a source electrode and drain electrode arranged on [one] the major surface of said substrate to face each other via said gate electrode; and

an insulating film [formed on a] covering bottom [surface] and [a] side [surface] surfaces of each of said gate electrode and said gate wiring layer; and

wherein said gate electrode, said gate wiring layer, said source electrode, and said drain electrode have upper surface levels equal to or lower than an upper surface level of said device isolation insulating film.

31. (Amended) A device according to claim 30, further comprising a source diffusion layer and a drain diffusion layer below said source electrode and said drain electrode [of said substrate].

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

36. (Amended) A device according to claim 30, further comprising a connection wiring layer connected to at least one of said source electrode, said drain electrode, said gate electrode, and said gate wiring layer [on one major surface of said substrate], said connection wiring layer having an upper surface level equal to or lower than the upper surface level of said device isolation insulating film.

37. (Amended) A semiconductor device comprising:

a substrate;

a gate wiring layer formed on one major surface of said substrate;

an insulating film [formed] interposed between said substrate and said gate wiring layer and [on] covering a side surface of said gate wiring layer;

a pair of thin films formed by epitaxial growing a semiconductor on one major surface of said substrate, and arranged on two sides of said gate wiring layer; and

a gate sidewall formed on said pair of thin films, covering said side surface of said gate wiring layer, and made of an insulator.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com